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a first impurity region having the n-type conductivity which forms a source region or a drain region, wherein the first impurity region is not overlapped with the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region and a fifth impurity region having p-type conductivity which forms a source region or a drain region; and

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region overlapped with a gate electrode; and
a fourth impurity region having the n-type conductivity and a first impurity region having the n-type conductivity which forms a source region or a drain region, wherein the first impurity region and the fourth impurity region are not overlapped with the gate electrode, wherein an impurity element having the n-type conductivity is included in the third impurity region and in the fourth impurity region and a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

9. (Twice Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:

a) said driver circuit comprises:

a first thin film transistor comprising:

a channel forming region and a third impurity region having n-type conductivity, wherein the channel forming region and the third impurity region are overlapped with a gate electrode; and

a first impurity region having the n-type conductivity which forms a source region or a drain region, wherein the first impurity region is not overlapped with the gate electrode;

a second thin film transistor comprising:

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a channel forming region and a third impurity region having the n-type conductivity, wherein the channel forming region and the third impurity region are overlapped with a gate electrode; and

a second impurity region having the n-type conductivity and a first impurity region having the n-type conductivity which forms a source region or a drain region, wherein the first impurity region and the second impurity region are not overlapped with the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region and a fifth impurity region having p-type conductivity which forms a source region or a drain region; and

b) said pixel section comprises:

a fourth thin film transistor having:

a channel forming region overlapped with a gate electrode; and

a fourth impurity region having the n-type conductivity and a first impurity region having the n-type conductivity which forms a source region or a drain region, wherein the first impurity region and the fourth impurity region are not overlapped with the gate electrode.

18. (Twice Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:

a) said driver circuit comprises:

a third thin film transistor comprising:

a channel forming region overlapped with a gate electrode; and

a second impurity region having n-type conductivity and a first impurity region having the n-type conductivity which forms a source region or a drain region, wherein the first impurity region and the second impurity region are not overlapped with the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region and a fifth impurity region having p-type conductivity which forms a source region or a drain region; and

b) said pixel section comprises:

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a fourth thin film transistor comprising:
a channel forming region overlapped with a gate electrode; and
a fourth impurity region having the n-type conductivity and a first impurity region the n-type conductivity which forms a source region or a drain region, wherein the first impurity region and the fourth impurity region are not overlapped with the gate electrode,
wherein the gate electrode has a first layer comprising TaN and a second layer comprising Ti on the first layer.

27. (Twice Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:
a) said driver circuit comprises:
a first thin film transistor comprising:
a channel forming region and a third impurity region having n-type conductivity, wherein the channel forming region and the third impurity region are overlapped with a gate electrode;
and
a first impurity region having the n-type conductivity which forms a source region or a drain region wherein the first impurity region is not overlapped with the gate electrode;
wherein said first thin film transistor constitutes a shift register circuit, and
a second thin film transistor comprising:
a channel forming region and the third impurity region having the n-type conductivity, wherein the channel forming region and the third impurity region are overlapped with a gate electrode; and
a second impurity region having the n-type conductivity and a first impurity region having the n-type conductivity which forms a source region or a drain region, wherein the first impurity region and the second impurity region are not overlapped with the gate electrode;
wherein said second thin film transistor constitutes a sampling circuit, and
b) said pixel section comprises:
a fourth thin film transistor comprising: